A 902-928 MHz PLL Design and Simulation for Biomedical Applications

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***Abstract*—Today radio frequency (RF) Link is widely used as the intermediate between the sensor unit and the computer for bio-medical applications, mostly in the area of muscular stimulation (for heart or limbs diseases) and of cortical or nerve stimulations (for blind or partially blind people or hearing diseases).**

The RF link is acted as the isolation between the user and computer where the system consists of a transmitter and a receiver with a transmission link in between. In case of unforeseen failure of the computer, the current which are used to power the computer will not be able to reach the end user directly. Therefore, the RF link protects the end user from possible injuries. The frequencies of operation were chosen to be in the range of 902-928 MHz or industrial, scientific and medical radio band (ISM) band.

A phase-locked loop (PLL) is one of the critical devices in modern RF biomedical systems; it is used to generate stable output high frequency signals from a fixed low-frequency signal in both end of the system. The design of PLL tuning range should be stretched to accommodate conditions that would affect frequency.

In this paper a high accuracy low noise 3rd order PLL for the ISM band is designed, CppSim simulation is used to confirm the theoretical background and successful circuit operation.

***Keywords*— 3rd order PLL, ISM band, CppSim.**

I. INTRODUCTION

PLLs are used extensively in the area of communication, computer, and biomedical systems. In most modern biomedical systems, different version of the clock is required at a different frequency/phase than the reference; in this case a PLL is the essential design element to create the required signal with different tuning frequencies [1].

The PLL basically consist of a phase frequency detector (PFD), a loop filter (LF), and a voltage controlled oscillator (VCO). It is function is to adjust the frequency/Phase of the VCO produced signal to the frequency/phase of the reference or input signal. A simplified PLL block diagram is shown in figure 1 [2].

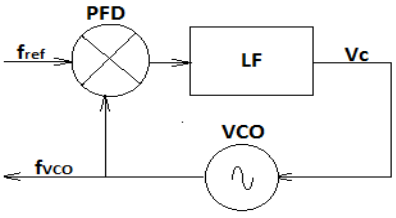

Fig. 1 The PLL simplified block diagram

The PFD compares the frequency/phase of the f_{ref} with the f_{VCO}, the difference voltage is passed through a loop filter (LF) and then applied to the VCO control voltage. The feedback loop is trying to adjust the VCO voltage so that the two compared signals have the same frequency and phase.

With the rapid expansion of the wireless/RF biomedical systems, there has been a proliferation to design the next winning wireless connectivity product to cover the frequency range. So, the design of a PLL circuit for wireless communication transceiver becomes an important and essential subject to study [3].

There are some popular references in this area. In [4] A. Rofougaran et. al. presents first monolithic CMOS RF transmitter, which is part of a complete low-power transceiver operating in the 902-928 MHz ISM frequency band, they integrated all PLL element in a 1μm-CMOS IC. The design of a PLL for a wide frequency including one VCO of low power and small chip area is proposed in [5]. In [6] an exact analysis for 3rd order charge-pump phase-locked loops using state equations is presented. Finally T. H. Lin et al. in [7] proposes a novel charge pump (CP) circuit and a gated-offset linearization technique to improve the performance of a delta sigma fractional-N PLL that enables the PFD/CP system to operate at an improved linear region.

This paper presents design and simulation of the 3rd order 902-928 MHz PLL to generate the RF signals required for both up conversion and down-conversion of biomedical transceivers, the major basic requirements in this design are to achieve the performance goals of low phase noise, low spurious output and to step, or hop, from one frequency to another in a specified period of time.

II. THE 3RD ORDER PLL BASICS

The biomedical wireless RF transceiver, requires a stable band of RF frequency to up/down convert the generated or reference frequency using a calibration or PLL circuit.

To improve the usable ISM band performance. The third order PLL gives the following advantages; low phase noise, more design freedom, superior noise rejection, and lower steady state error.

The VCO will have an input capacitance in combination with a resistor; this becomes an issue in 3rd order PLL designs. Based on the use of a basic passive two pole Loop filter with a single-pole spur filter of VCO, the standard 3rd order loop filter configuration of the PLL is shown in figure 2.

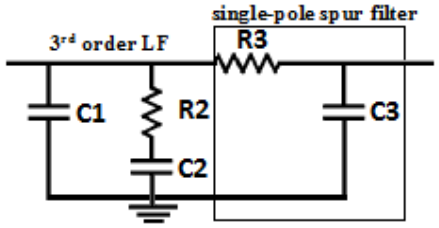

Fig. 2 The combined 3rd order LF with a single-pole spur filter configuration

The design of a 3rd order PLL typically involves determining the type of loop filter, selecting the proper ISM bandwidth, and establishing the desired stability. Therefore, according to design calculations the elements values can be determined to achieve the expected performance limit [8]. This comprises a second order filter section, and an R_1C_1 section providing an extra pole to assist the attenuation of the sidebands at multiples of the comparison frequency that may appear. So, the input signal f_{ref} and f_{VCO} will be tuneable in a stable state.

The system model of the 3rd order charge pump PLL is shown in figure 3. The charge pump (CP) always used to convert produced digital pulses from PFD into an analogue current that is converted to a voltage via the passive loop filter.

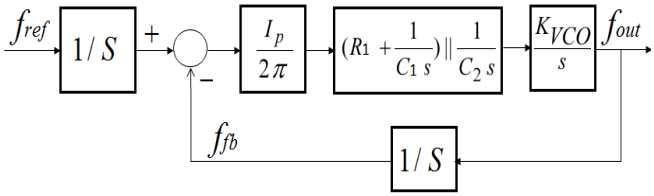

Fig. 3 The system model of the 3rd order PLL

The open and closed loop transfer functions are given in equations 1 and 2 respectively [9] [10].

$$H(S)_{open} = K_v \frac{R_2C_2S + 1}{S^2[\frac{R_2C_2}{1+(C_2/C_1)}S + 1]} \quad (1)$$

$$H(S)_{close} = S^3 + \frac{1+(C_2/C_1)}{R_2C_2}S^2 + K_v(1+\frac{C_2}{C_1})S + \frac{K_v(1+\frac{C_2}{C_1})}{R_2C_2} \quad (2)$$

Therefore, according to equations 1&2, and the availability of sufficiently fast processing, it is possible to develop and design 3rd order PLLs using CppSim simulation program. The design procedure presents the 3rd order PLL that is reduced spur levels applicable for most RF biomedical systems.

III. The 3rd Order PLL Design

The designing of the 3rd order phase locked loop (PLL) to be operated at the range of 902-928MHz required investigation of the parameters on timing model including several common noise sources.

The fully integrated ADF9010 [11] which is the preferred chip in this design operates in the frequency range from 840MHz up to 960MHz. Figure 4 shows the circuit diagram of the 3rd order PLL using ADF9010 chip.

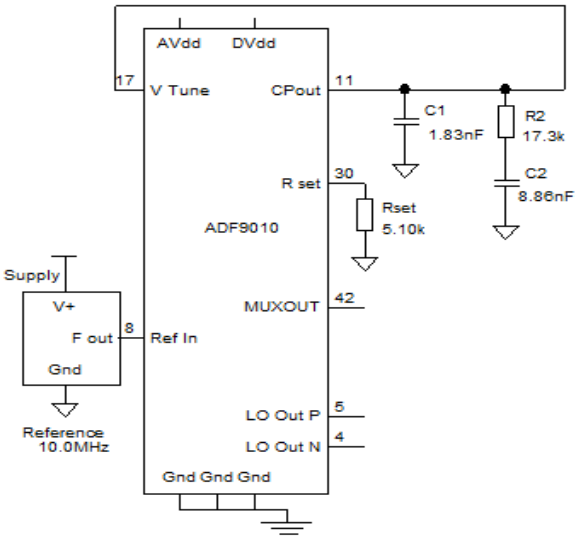

Fig. 4 The 3rd order PLL circuit diagram using ADF9010 chip

The 3rd order PLL of figure 4 was designed and simulated using the following parameters:

- PLL Chip is ADF9010 including VCO,
- The Reference is custom
- VCO Divider Outside Loop: division ratio = 4
- Frequency Domain Analysis of PLL
- Analysis at PLL output frequency of 914.90625MHz.
- Phase Noise Data (table 1)

TABLE I
PHASE NOISE DATA

Freq (Hz)	Total (dBc/Hz)	VCO (dBc/Hz)	Chip (dBc/Hz)	Filter (dBc/Hz)
100	-66.25	-66.31	-84.72	-110.4
1.00k	-63.87	-63.94	-82.64	-91.16
10.0k	-90.49	-90.97	-110.4	-106.8
100k	-120.0	-120.0	-141.2	-146.5
1.00M	-141.9	-141.9	-181.2	-186.5

- Phase jitter using brick wall filter from 10.0kHz to 100kHz, Phase Jitter 0.17 degrees rms.
- Transient Analysis of PLL, Frequency change from 902MHz to 928MHz, Simulation runs for 2.21ms.
- Frequency Locking, Time to lock to 1.00kHz is 1.01ms, Time to lock to 10.0 Hz is 1.44ms.
- Phase Locking (VCO Output Phase), Time to lock to 10.0 deg is 998μs; Time to lock to 1.00 deg is 1.18ms.

IV. Simulation Results

The complete circuit diagram of figure 4 was simulated for the range of 902-928MHz ISM frequency band which are applicable in wireless biomedical systems. Figures below (from 5 to 15) show samples of the resultant plots.

Figures 5,6, and 7 shows components simulation results.

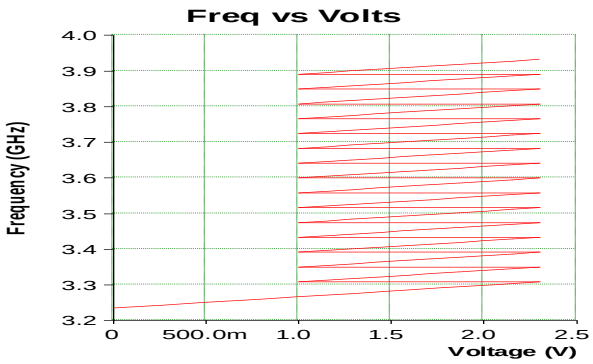

Fig. 5 The VCO frequency vs volts relationship

Figure 5 shows that the VCO constant K_o is specified at 12MHz/V, and the tuning is in the range of 902-928MHz.

Figure 6 shows the VCO phase noise at 915MHz measured in a free running configuration.

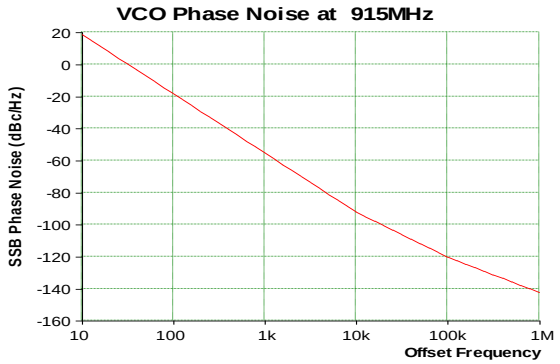

Fig. 6 The VCO phase noise at 915MHz

Figure 7 shows the phase noise from the reference source. The reference phase noise affects the output phase noise of the PLL, primarily inside the loop bandwidth.

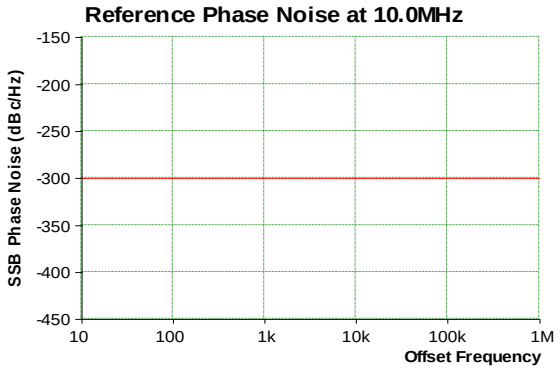

Fig. 7 The reference phase noise at 10MHz

Figures 8,9, and 10 shows frequency domain simulation results. The frequency domain plots contains the setup data for the frequency analysis (loop gain / phase, and phase noise).

The PLL open loop gain (amplitude and phase) are shown in figure 8, while figure 9 represent the amplitude and phase of the closed loop gain of the PLL, both determined at the analysed frequency.

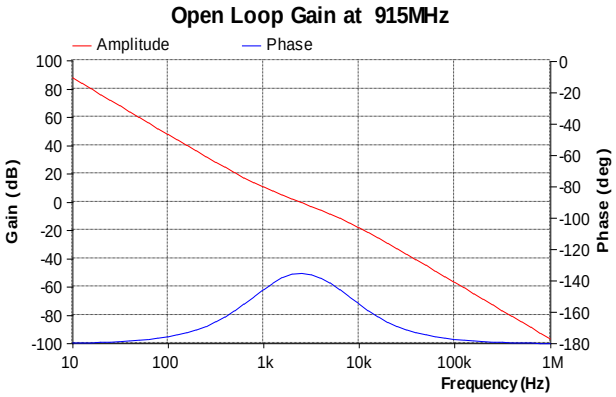

Fig. 8 The open loop gain at 915MHz (amplitude and Phase)

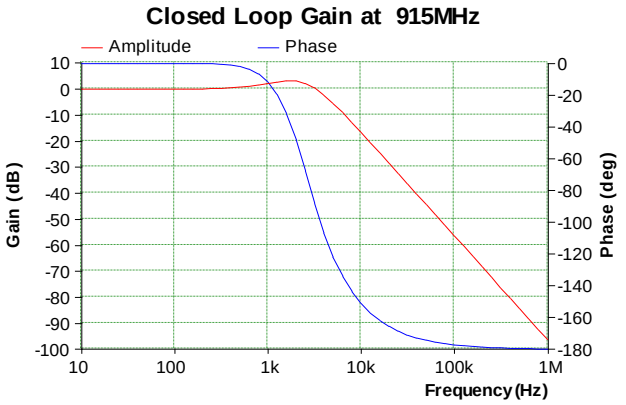

Fig. 9 The closed loop gain at 915MHz (amplitude and Phase)

Plot of figure 10 represents the phase noise from the VCO measured when locked occurred in the PLL. This includes all noise sources within the PLL.

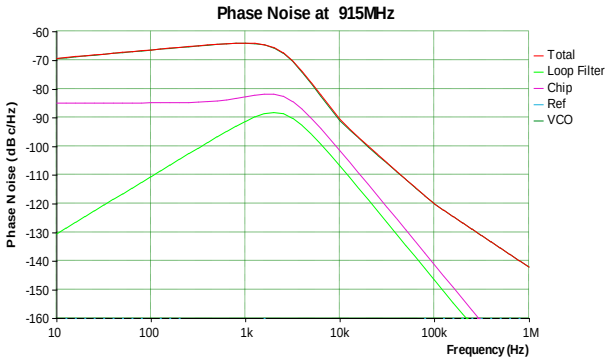

Fig. 10 The PLL phase noise at 915MHz

Figures 11, 12, 13, 14, and 15 shows the time domain simulation results. Figure 11 shows the variation of the PLL output frequency under transient conditions. The frequency error of the PLL during transient conditions is shown in fig 12.

Figure 13 shows the output phase error of the PLL during transient conditions (the phase error at the output of the VCO). The lock detect output during transient conditions is represented in figure 14. The output of the PLL phase detector during transient conditions is shown in figure 15.

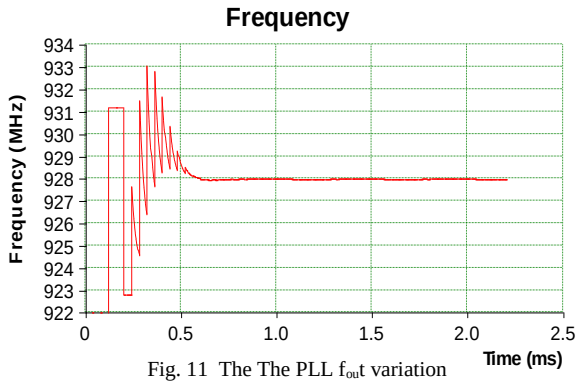

Fig. 11 The The PLL f_{out} variation

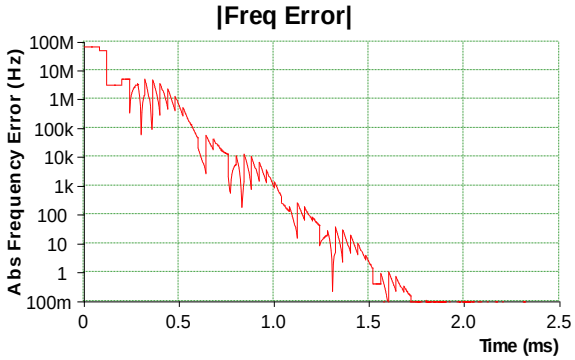

Fig. 12 The PLL frequency error

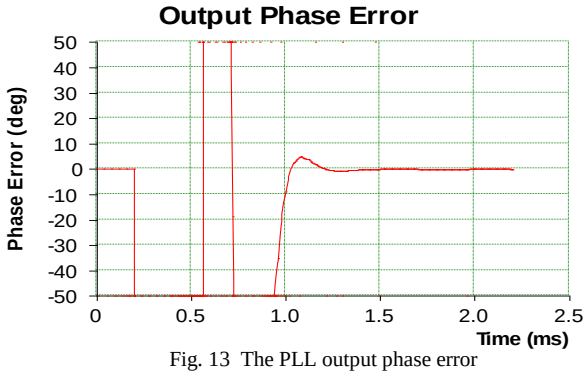

Fig. 13 The PLL output phase error

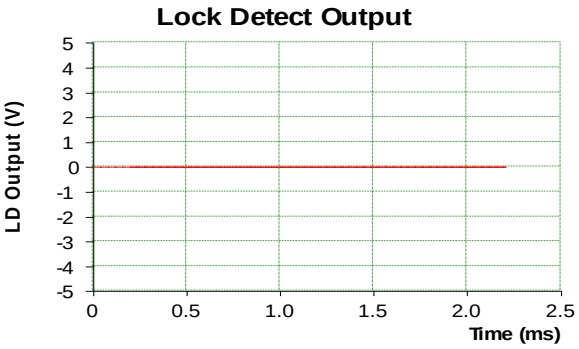

Fig. 14 The PLL lock detect output

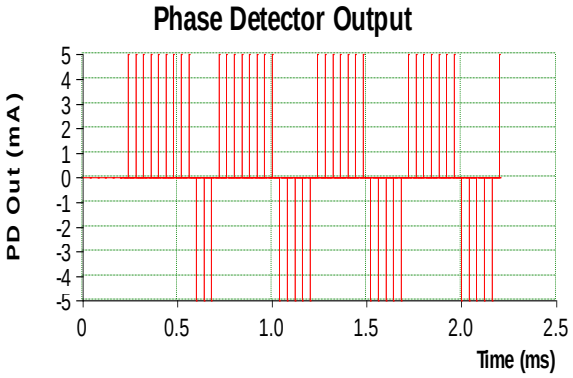

Fig. 15 The PLL phase detector output

The purpose of using CppSim simulation software is to introduce a 3rd order PLL that is specifically designed and simulated. The result verifies that, the PLL can step from one frequency to another in the range 902-928MHz for ISM in many current biomedical applications. The CppSim enables and allows the rapid determination of switching speed of PLL circuits. It is used to evaluate the effect of varying design parameters, such as loop bandwidth and phase margin on the lock time by altering the requested parameters and studding transient performance in the time domain instantaneously, as well as sensitivity investigation of the lock time to component values can be considered. It is clear that, the simulation is fast in time and frequency domain, as well as the characteristics and simulation of the PLL components, and the results are agree with the pre-calculated values.

V. Conclusions

Interface to RF radio transceivers; always produce problems in biomedical wireless devices. Therefore, these problems in recent years make researchers to study and work toward the design of appropriate and reasonable PLLs applicable for ISM frequency band.

In this paper, the 3rd order PLL is designed and simulated for 902-928MHz ISM frequency band using a ADF9010 chip as a full y integrated RF modulator.

The design procedure verifies a high accuracy in progress, and can significantly improve the PLL circuits in most biomedical applications.

The simulation of the transient model includes important non-linear effects such as phase detector cycle slipping, phase detector saturation, active filter limiting and VCO tuning law of curvature. It is possible to study and demonstrate these effects and evaluate their significance. The CppSim simulation program shows the satisfactory results of this study.

Therefore, design and simulation of the 3rd order PLL using ADF9010 chip can be considered as a critical design parameter in current and future biomedical devices and systems for RF-ISM band, and illuminates the way to new research in the field.

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APPENDIX (ADF9010)

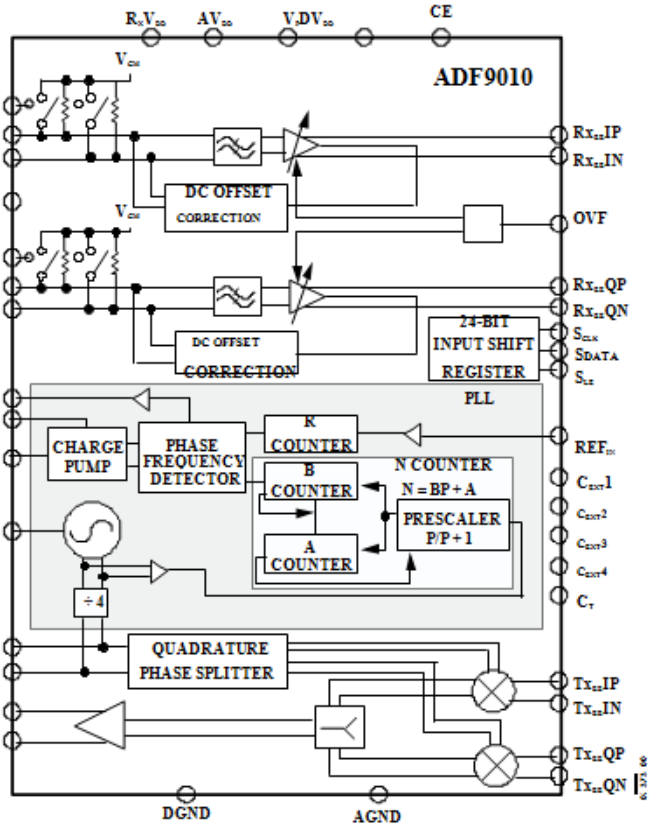
FEATURES

- 840 MHz to 960 MHz ISM bands
- Rx baseband analog low-pass filtering and PGA
- Integrated RF Tx upconverter
- Integrated integer-N PLL and VCO
- Integrated Tx PA preamplifier
- Differential fully balanced architectures
- 3.3 V supply
- Low power mode: <1 mA power-down current
- Programmable Rx LPF cutoff
  - 330 kHz, 880 kHz, 1.76 MHz, and bypass
- Rx PGA gain settings: 3 dB to 24 dB in 3 dB steps
- Low noise BiCMOS technology
- 48-lead, 7 mm × 7 mm LFCSP

ADF9010 APPLICATIONS

- 900 MHz RFID readers
- Unlicensed band 900 MHz applications

ADF9010 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADF9010 is a fully integrated RF Tx modulator and Rx analogue baseband front end that operates in the frequency range from 840 MHz to 960 MHz. The receive path consists of a fully differential I/Q baseband PGA, low-pass filter, and general signal conditioning before connecting to an Rx ADC for baseband conversion. The Rx LPF gain ranges from 3 dB to 24 dB, programmable in 3 dB steps. The Rx LPF features four programmable modes with cutoff frequencies of 330 kHz, 880 kHz, and 1.76 MHz, or the filter can be bypassed if necessary.