Design of The Feedback Controller (PID Controller) for The Buck Boost Converter

1)Sattar Jaber Al-Isawi 2) Ehsan A. Abd Al-Nabi
Department of Electromechanical Eng.
The High Institute for Industry-Libya-Misrata
sattarjaber@yahoo.com

ABSTRACT

The aim of this paper is to design a best compensator for the buck-boost converter system operates in a continuous conduction mode. The small signal of the buck boost is derived first to find the line-to-output and control-to-output transfer functions which they help to design the feedback controller and help in the study of the system stability.

key words: Converter, Control, Switching

1.Introduction

In all switching converters, the output voltage $V_o(t)$ is a function of the line voltage $V_i(t)$, the duty cycle d(t), and the load current $i_{Load}(t)$, as well as the converter circuit element values. In a dc-dc converter application, it is desired to obtain a constant output voltage Vo(t)=Vo, in spite of disturbances in $V_i(t)$ and $i_{Load}(t)$, and in spite of variations in the converter circuit element values[1,2]. The sources of these disturbances and variations are many, the input voltage of an off-line power supply may typically contain periodic variations at the second harmonic of the ac power system frequency (100Hz or 120Hz), produced by a rectifier circuit. [3,4]. The magnitude of vi(t) may also vary when neighboring power system loads are switched on or off. The load current $i_{Load}(t)$ may contain variations of significant amplitude, and a typical power supply specification is that the output voltage must remain within a specification range when the load current take a step change form. The values of the circuit elements are constructed to a certain tolerance, and so in high volume manufacturing of a converter, converters are constructed whose output voltages lie in some disturbances [5,6].

2. Small Signal Model

To derive the small signal model for the buck boost converter we have to follow the procedure below:

t_{on} Interval .

During the subinterval (1) when the switch ON shown in Fig.(1) .

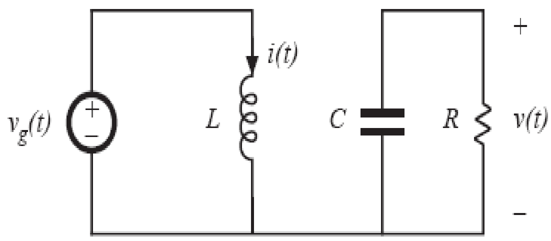

Fig.(1) subinterval (1)

The inductor voltage and capacitor current are:

$$vL(t) = L * \frac{diL(t)}{dt} = vi(t) \quad \text{.........(1)}$$

$$ic(t) = C * \frac{dvo(t)}{dt} = -\frac{vo(t)}{R} \quad \text{.........(2)}$$

Small ripple approximation: replace waveforms with their low frequency averaged values.

$$vL(t) = L * \frac{diL(t)}{dt} = \langle vi(t) \rangle \quad \text{.........(3)}$$

$$ic(t) = C * \frac{dvo(t)}{dt} = -\frac{\langle vo(t) \rangle}{R} \quad \text{.........(4)}$$

t_{off} Interval

During the subinterval (2) when the switch OFF shown in Fig.(2).

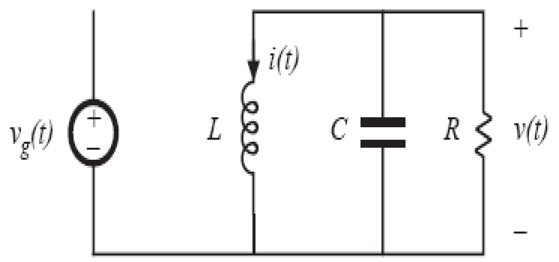

Fig.(2) subinterval (2)

Inductor voltage and capacitor current are:

$$vL(t) = L * \frac{diL(t)}{dt} = vo(t) \text{ ....(5)}$$

$$ic(t) = C * \frac{dvo(t)}{dt} = -iL(t) - \frac{vo(t)}{R} \text{ ....(6)}$$

Small ripple approximation: replace waveforms with their low frequency averaged values.

$$vL(t) = L * \frac{diL(t)}{dt} = \langle vo(t) \rangle \text{ ....(7)}$$

$$ic(t) = C * \frac{dvo(t)}{dt} = -\langle iL(t) \rangle - \frac{\langle vo(t) \rangle}{R} \text{ ....(8)}$$

Averaged the inductor waveforms

$$\langle vL(t) \rangle = d(t) * \langle vi(t) \rangle - d'(t) * \langle vo(t) \rangle \text{ ....(9)}$$

$$L * \frac{d\langle iL(t) \rangle}{dt} = d(t) * \langle vi(t) \rangle + d'(t) * \langle vo(t) \rangle \text{...(10)}$$

Averaged the capacitor waveforms

$$\langle ic(t) \rangle = d(t) * [-\frac{\langle vo(t) \rangle}{R}] + d'(t) * [-\langle iL(t) \rangle - \frac{\langle vo(t) \rangle}{R}] \text{................................(11)}$$

…

$$C * \frac{d\langle vo(t) \rangle}{dt} = -d'(t) * \langle iL(t) \rangle - \frac{\langle vo(t) \rangle}{R} \text{ ....(12)}$$

Averaged the input current

$$i_i(t) = \begin{cases} iL(t) & during\,sub\,\text{int}\,erval - (1) \\ 0 & during\,sub\,\text{int}\,erval - (2) \end{cases}$$

The averaged value is :

$$\langle i_i(t) \rangle = d(t) * \langle i_i(t) \rangle \text{ ....(13)}$$

The converter averaged equations are:

$$L * \frac{d\langle iL(t) \rangle}{dt} = d(t) * \langle vi(t) \rangle + d'(t) * \langle vo(t) \rangle \text{..(14)}$$

$$C * \frac{d\langle vo(t) \rangle}{dt} = -d'(t) * \langle iL(t) \rangle - \frac{\langle vo(t) \rangle}{R} \text{ ......(15)}$$

$$\langle i_i(t) \rangle = d(t) * \langle i_i(t) \rangle \text{ ....(16)}$$

where, d'(t)=1-d(t)

These equations are non-linear.

By considering a certain steady state values and add a small a.c variation (the a.c component are very small), the above equations become:

$$L * \frac{d(IL + i\hat{L}(t))}{dt} = (D + \hat{d}(t)) * (Vi + v\hat{i}(t)) + (D' - d'(t)) * (Vo + v\hat{o}(t)) \text{.........................(17)}$$

The d.c terms equal zero, and the second order ac terms are small values and can be neglected.

$$L * \frac{di\hat{L}(t)}{dt} = D * v\hat{i}(t) + \hat{d}(t) * (Vi - Vo) * n + D' * v\hat{o}(t) \text{...(18)}$$

The a.c equivalent circuit of the above equation is shown in Fig.(3).

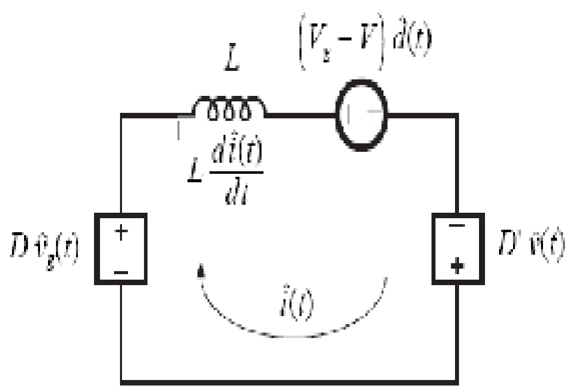

Fig.(3) The a.c equivalent circuit of inductor loop.

To linearize the capacitor equation:

$$C*\frac{d(Vo+v\hat{o}(t))}{dt}=-(D'-d'(t))*(IL+i\hat{L}(t))-\frac{(Vo+v\hat{o}(t))}{R}\text{.......................................(19)}$$

The d.c terms equal zero, and the second order ac terms are small values and can be neglected.

$$C*\frac{v\hat{o}(t)}{dt}=-D'*i\hat{L}(t)-\frac{v\hat{o}(t)}{R}+Io*\hat{d}(t)\text{ .(20)}$$

The a.c equivalent circuit of the above equation is shown in Fig(4).

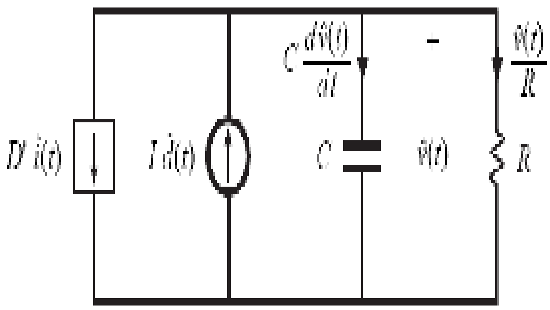

Fig.(4)The a.c equivalent circuit of capacitor node

To linearize the input current:

$$(Ii+\hat{i}_i(t))=(D+\hat{d}(t))*(IL+\hat{i}_L(t))\text{ ....(21)}$$

The d.c terms equal zero, and the second order ac terms are small values and can be neglected.

$$\hat{i}_i(t)=D*i\hat{L}(t)+n*\hat{d}(t)*IL\text{ ....(22)}$$

The a.c equivalent circuit is shown in Fig.(5)

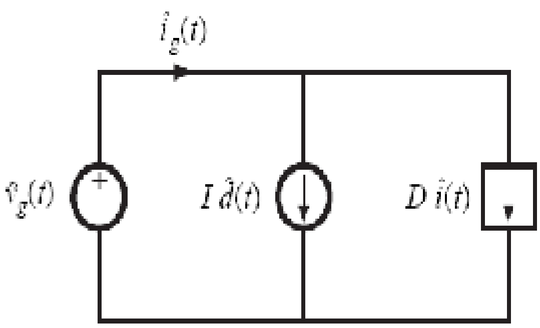

Fig.(5) The a.c equivalent circuit of the input port.

3. Transfer Functions of Buck Boost Converter

The small signal change in the output voltage of the converter can be represented as follows:

$$v\hat{o}(s)=Gvi(s)*v\hat{i}(s)+Gvd(s)*\hat{d}(s)\text{.......(23)}$$

where,

$$Gvi(s)=\frac{v\hat{o}(s)}{v\hat{i}(s)}\Big|_{\hat{d}=0}\text{..............................(24)}$$

$$Gvd(s)=\frac{v\hat{o}(s)}{v\hat{d}(s)}\Big|_{v\hat{i}=0}\text{.............................(25)}$$

By solving the small signal model we can get these transfer functions as follows:

$$Gvi(s)=-\frac{D}{D'}\frac{1}{1+\frac{sL}{D'^2R}+\frac{s^2LC}{D'^2}}\text{ ....(26)}$$

$$Gvd=-\frac{Vi-Vo}{D'}*\frac{R\Uparrow\frac{1}{sC}}{\frac{sL}{D'^2}+R\Uparrow\frac{1}{sC}}+IL*(\frac{sL}{D'^2}\Uparrow R\Uparrow\frac{1}{sC})\text{..............................(27)}$$

4. Effect of Negative Feedback

The block diagram which models the small-signal ac variation of the complete system of the converter is as shown in Fig.(6) below:

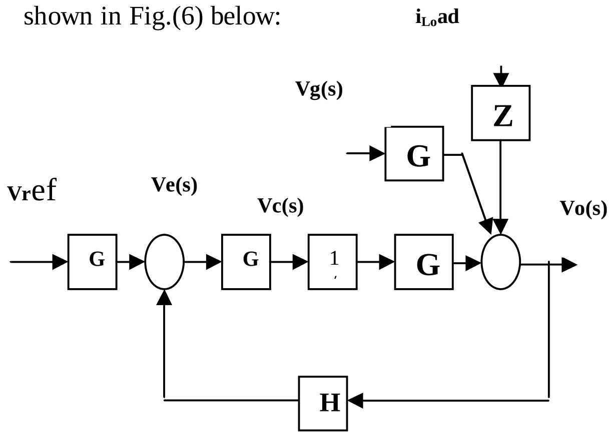

Fig.(6) Block diagram which models the small-signal ac variation of the complete system of the converter.

The formula of output voltage variation that represents the effect of the feedback control on the system is as follows:

$$v\hat{o}(t) = vr\hat{ef}(t) * \frac{1}{H(s)} \frac{T}{1+T} + v\hat{i}(t) * \frac{Gvi(s)}{1+T}$$

$$+ \frac{-\hat{i}Load * Zout}{1+T} \text{……………………………(28)}$$

where,

$$T(s) = \frac{H(s) * Gc(s) * Gvd(s)}{VM} \text{……………..(29)}$$

From equation (28) it is very clear that the change of the reference voltage, input voltage and load current depend on a certain transfer functions T/(1+T) and 1/(1+T). These transfer functions are very important in the design of the compensator.

5.Controller Design

A Combined PID compensator will be used to control the dc-dc Buck-Boost converter system.

The first step is to select the feedback gain H(s). The gain H is chosen such that the regulator produces a regulated -15V dc output. Let as assume that we will succeed in designing a good feedback system, which causes the output voltage to accurately follow the reference voltage. This is accomplished via a large loop gain T(s), which leads to a small error voltage: ve ≈ 0. Hence, Hv=vref. So we should choose :

$$H(s) = \frac{Vref}{Vo} = \frac{5}{15} = \frac{1}{3}$$

The quiescent duty cycle is given by the steady-state solution of the converter:

$$Vo = -Vs * \frac{D}{1-D}$$

by inserting the input and output voltages, we can find the duty cycle:

$$-15 = -48 * \frac{D}{1-D} \Rightarrow D = 0.238$$

$$D' = 1 - D = 1 - 0.238 = 0.762$$

The quiescent value of the control voltage, Vc, will be equal:

Vc=D*VM

Vc=0.238*3=0.714V

Thus, the quiescent conditions of the system are known. It remains to design the compensator gain Gc(s).

The open loop converter normalized transfer functions derived from the small signal model is:

$$Gvd(s) = Gdo * \frac{(1 - \frac{s}{wz})}{1 + (\frac{s}{Qo * wo}) + (\frac{s}{wo})^2} \text{……(30)}$$

$$Gvi(s) = Gio * \frac{1}{1 + (\frac{s}{Qo * wo}) + (\frac{s}{wo})^2} \text{……...(31)}$$

$$|\ Gio\ | = \frac{D}{D'} = \frac{0.238}{0.762} = 0.3123$$

$$|\ Gdo\ | = \frac{Vo}{D * D'} = \frac{15}{0.238 * 0.762} = 82.71$$

$$wo = \frac{D'}{\sqrt{L*C}} = \frac{0.762}{\sqrt{50*10^{-6} * 220*10^{-6}}} = 7265.3$$

$$fo = 1.156 KHz$$

$$Qo = D' * R * \sqrt{\frac{C}{L}} = 7.99 = 18 \quad dB$$

$$wz = \frac{D'^2 * R}{D * L} = 243968 \quad rad/\sec \Rightarrow$$

$$fo = 38.828 \quad KHz$$

By using the above equation, The loop gain of the system is:

$$T(s) = Gc(s) * (\frac{1}{VM}) * Gvd(s) * H(s) \text{……(32)}$$

or

$$T(s) = \frac{Gc(s) * H(s) * Gdo}{VM} \frac{(1 - \frac{s}{wz})}{1 + (\frac{s}{Qo * wo}) + (\frac{s}{wo})^2} \text{……...(33)}$$

The uncompensated loop gain Tu(s), with unity compensator gain Gc(s)=1, is:

$$Tu(s)=\frac{H(s)*Gdo}{VM}\frac{(1-\frac{s}{wz})}{1+(\frac{s}{Qo*wo})+(\frac{s}{wo})^2} \quad .....(34)$$

where the dc gain is:

$$Tuo=\frac{H*Gdo}{VM}=\frac{0.334*82.71}{3}=9.18=19.257\ dB$$

The uncompensated loop gain has a crossover frequency of approximation 3.2 kHz with phase margin ≈ 0 degree. In this paper, we will design a compensator to attain a crossover frequency of fc=10kHz, or one twentieth of the switching frequency. The uncompensated loop gain has a magnitude at 10 kHz equal to ≈-18 dB. In addition the compensator should improve the phase margin, since the phase of the uncompensated loop gain is nearly -220 degree at 10KHz. So a PD compensator is needed. According to the relation between the phase margin and the Q-factor, we will select the phase margin equal to 52 degree to get Q-factor equal to 1. With fc=10KHz and ϴ=52 degree, leads to the following compensator pole and zero frequencies:

$$fz1=(10KHz)*\sqrt{\frac{1-\sin(52)}{1+\sin(52)}}=3.442KHz$$

$$fp=(10KHz)*\sqrt{\frac{1+\sin(52)}{1-\sin(52)}}=29KHz$$

To obtain unity loop gain at 10 KHz and approximate the compensated loop gain by its high frequency, then the low frequency compensator gain must be:

$$Gco=(\frac{fc}{fo})^2*(\frac{1}{Tuo})*\sqrt{\frac{fz1}{fo}}=2.8=8.94\quad dB$$

The loop gain with the PD controller becomes:

$$T(s)=\frac{H(s)*Gdo}{VM}\frac{(1-\frac{s}{wz})*(1+\frac{s}{wz1})}{(1+\frac{s}{wp})*(1+(\frac{s}{Qo*wo})+(\frac{s}{wo})^2)} \quad ....(35)$$

The low frequency regulation can be further improved by addition of an inverted zero. A PID controller is then obtained. The compensator transfer function becomes:

$$Gc(s)=Gcm\frac{(1+\frac{s}{wz})*(1+\frac{wL}{s})}{(1+\frac{s}{wp})} \quad ....(36)$$

$$Gc(s)=2.8*\frac{(1+\frac{s}{21.626k})*(1+\frac{6.28k}{s})}{(1+\frac{s}{182.2k})}$$

The pole and zero fp and fz1 are unchanged. The midband gain (Gcm) is chosen to be the same as the previous (Gco). Hence, for frequencies greater than the fL, magnitude of the loop gain is unchanged by the inverted zero. The loop continues to exhibit a crossover frequency of 10 KHz. The frequency fL will chosen to be one-tenth of the cross over frequency, or 1 KHz. The inverted zero will then increase the loop gain at frequencies below 1KHz, improving the low frequency regulation of output voltage. With PID controller, the loop gain will be:

$$T(s)=\frac{H(s)*Gdo}{VM}\frac{(1-\frac{s}{wz})*(1+\frac{s}{wz1})*(1+\frac{wL}{s})}{(1+\frac{s}{wp})*(1+(\frac{s}{Qo*wo})+(\frac{s}{wo})^2)}$$

By doing many test for different crossover frequency, we found that increasing the cross over frequency more than 10K will reduce the phase margin and that will effect the stability of the system. It is found that when we design compensator for crossover frequency equal to 20kHz (10% of the switching frequency), the phase margin will be equal to 23 degree. Also, by putting the cross over frequency equal to 30KHz (15% of the switching frequency) the phase margin will be equal to 14 degree. The small value of the phase margin (in T(s)) cases the close loop transfer functions (1/(1+T)) and (T/(1+T)) to exhibit resonant poles with high Q. The system transient response exhibit overshoot and ringing. As the phase margin is reduce these characteristics become worst (higher Q, longer ringing) until the system becomes unstable.

From the previous figures of bode plots, we can see that the loop gain at 120Hz is equal to 47 dB. This gain can be improved by increasing (fL); however, this would require redesign of the PD portion of the compensator to maintain an adequate phase margin.

6. Simulation

A MATLAB/Simulink model is build to simulate the design of buck boost compensator which is designed before.

Fig.(7) and Fig.(8) show the output voltage versus the input voltage step change from 44V to 52V at 0.004s and from 52V to 44V at 0.005s. From these figures it is very clear that the controller respond very well under this change.

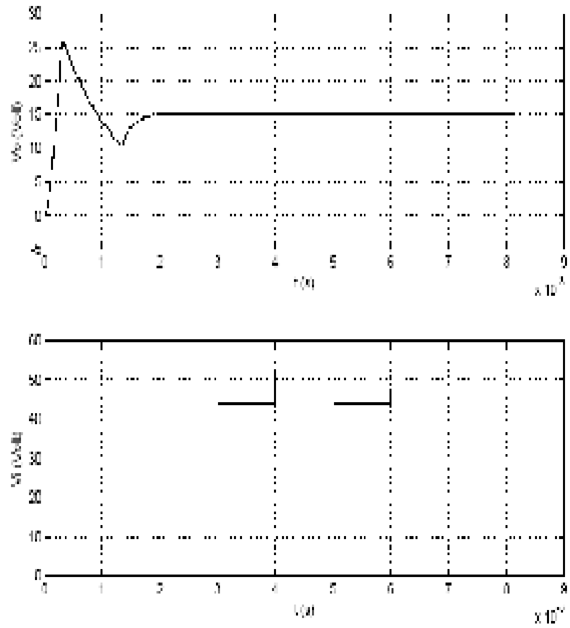

Fig.(7)Output voltage versus the input voltage step change from 44V to 52V at 0.004s and from 52V to 44V at 0.005s

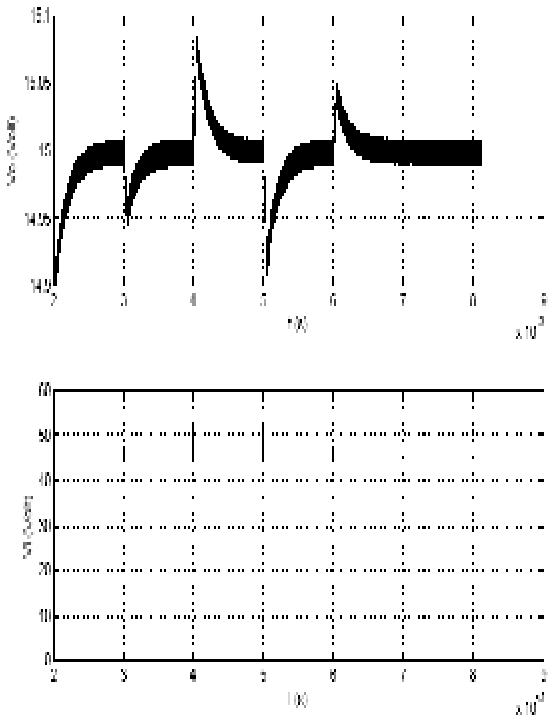

Fig.(8)Output voltage versus the input voltage step change from 44V to 52V at 0.004s and from 52V to 44V at 0.005s

The overshoot and the settling time for the input change from the 44V to 52V are equal to 0.5% and zero (according to the definition of ±2%, but if we just calculate the time till it become stable is equal to 0.5ms) respectively. The overshoot and the settling time for the input change from the 52V to 44V are equal to 0.5833% and zero (according to the definition of ±2% of the output signal, but if we just calculate the time till it become stable is equal to 0.5ms) respectively.

Fig.(9) and Fig.(10) show the output voltage versus the load step changes from 100% to 50% at 0.003s and from 50% to 100% at 0.006s. From these figures it is very clear that the controller respond very well under this change. The overshoot and the settling time for the load change from the 100% to 50% are equal to 0.66% and zero (according to the definition of ±2%, but if we just calculate the time till it become stable is equal to 0.1ms) respectively.

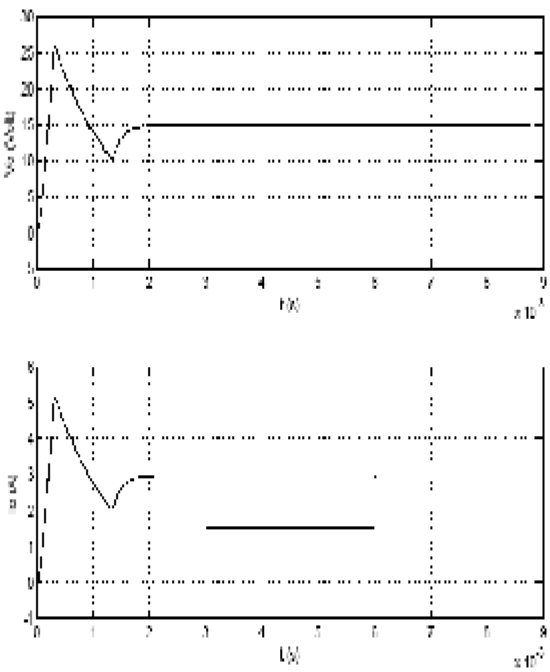

Fig.(9)The output voltage versus the load step changes from 100% to 50% at 0.003s and from 50% to 100% at 0.006s

The overshoot and the settling time for the load change from the 50% to 100% are equal to 0.8% and zero (according to the definition of ±2% of the signal, but if we just calculate the time till it become stable is equal to 0.1ms)respectively.

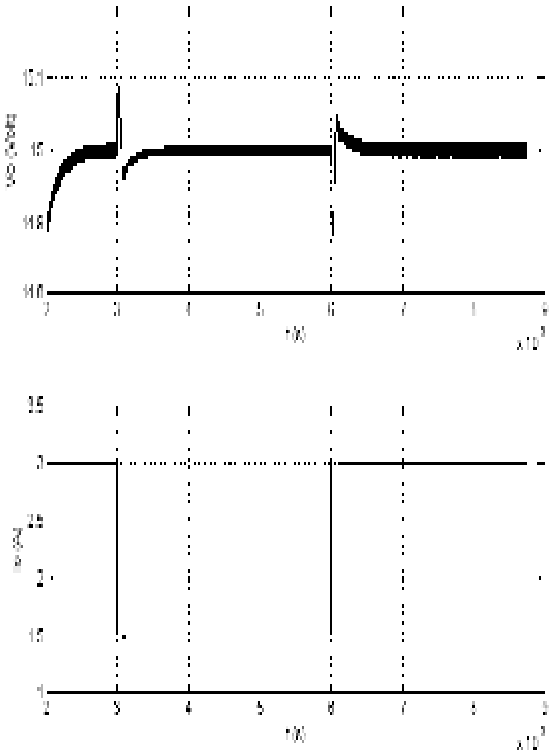

Fig.(10)The output voltage versus the load step changes from 100% to 50% at 0.003s and from 50% to 100% at 0.006s

Fig.(11) and Fig.(12) show the output voltage versus the voltage reference step changes from 0V to 5V at 0.001s and from 5V to 0V at 0.003s. From these figures it is very clear that the controller can not overcome the big change in the reference voltage. The overshoot and the settling time for the reference voltage change from the 0V to 5V are equal to 73% and 0.002s respectively. The overshoot and the settling time for the reference voltage change from the 5V to 0V are equal to zero and 0.0026s respectively.

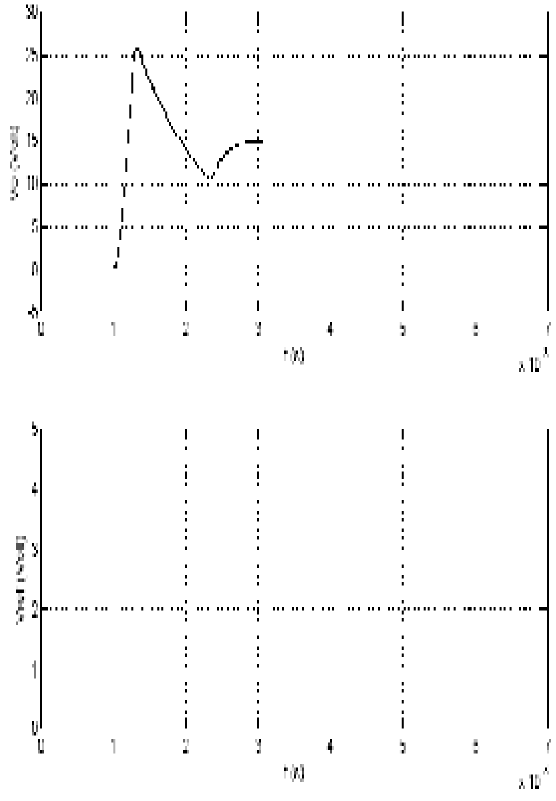

Fig.(11) Output voltage versus the voltage reference step changes from 0V to 5V at 0.001s.

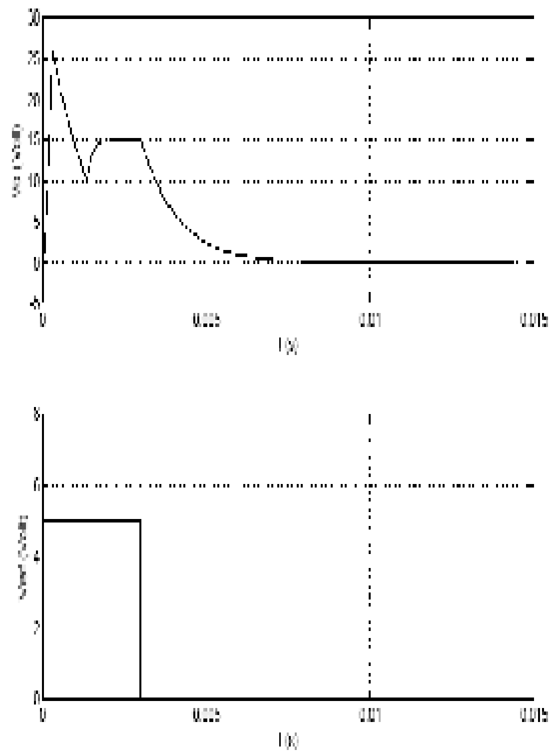

Fig.(12) Output voltage versus the voltage reference step changes from 5V to 0V at 0.003s.

7. Conclusion

In this paper a design of the feedback controller (PID controller) for the buck boost converter is done to get the best performance. A MATLAB/Simulink model is build to verify the performance of the compensator design. By applying large signal variation (for example by applying changes for the reference voltage from 0V to 5V) the system work fine but there is some overshoot and undershoot at the time of changes. Also, the compensator is test for changes in the input voltage and changes in the load. During these changes the system behaves very well with very less overshoot and settling time.

The PI compensator is used to increase the low frequency loop gain, such that the output is better regulated at d.c and at frequencies well below the loop crossover frequency. PD is used to increase the bandwidth of the feedback loop and to increase the phase margin at the crossover frequency. The crossover frequency (fz) is should be chosen to be successfully less than crossover frequency, such that an adequate phase margin is maintained.

References

[1].Sattar Jaber Al-Isawi , Ehsan A. Abd Al-Nabi "DESIGN A DISCRETE CONTROL SYSTEM OF PWM AC-AC CONVERTER", Drive",Proc. Of Int. UPEC, 2008.

[2].M.M.Hamada et al, "Harmonic Currents of Lighting Controllers (Dimmers)", 37th Int. UPEC ,2002

[3] H.P. Tiwari & R.A. Gupta, " Transient Behaviour of 12-Pulse Cycloconverter Fed Induction Motor Drive",Proc. Of Int. UPEC, pp. 700-704, 2002.

[4] A. K. Chattopadhayaya , " Cycloconverter Fed Drives: A Review", Journal of Indian Institute of scince,Vol.77 pp 397-419, Sept.-Oct., 1997.

[5].A.Kawamura, R. Chuaryapratip," Deadbeat Control of PWM Inverter with Modified Pulse Pattern for Unintirruptible Power Supply", IEEE Tran. On Ind. Elect. Vol 35 n0 2 1988.

[6] Collins & E. Randolph,"Torque and slip Behaviour of single phase induction motors driven from variable frequency supplies", IEEE Tran. on Ind., Appln.Vol.28, , May-Jaune, 1997.