# An Efficient Approach to Calculate Leakage Current Based on SPICEs Parameters at CMOS Transistors

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## ABSTRACT

The main idea of this paper is to discuss a new approach to optimize the value of leakage current in MOS transistors. It based on looking for optimal values of the main SPICE parameters which influence the value of the leakage current. These Values make in totally the leakage current, minimal value. The logic and the flow diagrams seem working correctly; various simulation results show the validity of the proposed technique and the value of the leakage is reduced finally as expected.

Key Words: Leakage Current, Low Power, Multithreshold Voltage, SPICE Parameters,

# 1. Introduction

The increasing demand for portable devices and hand held equipment now a day makes from low power design techniques to be first ordered. The mobile telephone, palmtops, laptops and recently the portable biomedical equipment are the most frequent devices which need always charge battery.

The resources of power dissipation at circuit level includes Dynamic Power Dissipation (DPD), Static Power Dissipation (SPD) and Leakage Current Power dissipation (LCP) are the main factors of power dissipation at portable devices. Various succeeded techniques are introduced and developed to reduce the dynamic and static power dissipation ignoring the value of the leakage power [1][2]. It happened because the value of the dynamic as well as static power were the main dominant resources of power dissipation (75% and 20%), while the value of the leakage current was in the minimal value (~ < 5%).

The motivation from μ-technology to nano-technology which caused a reduction in the supply voltage as well as in the threshold voltage is not only offering its own advantages of reducing both silicon area[3], dynamic power dissipation [4] as well as increasing the speed and the performance of the digital circuits [4], but it has its own disadvantage of increasing the value of the leakage current but also the complexity to calculate accurately the value of it.

## 2. Resources of Leakage current

Leakage current appeared recently as main factor of power dissipation, this is because the move from micro-technology to nano-technology which has as a result significant changes and scale in SPICE parameters such as threshold voltage, length of gate, gate dioxide thickness and supply voltage, all of these has a result to decrease dramatically the leakage current value.

Leakage current, which occurred in CMOS devices, categorized in two different parts: The dominant current sinks from the gate to the substrate of transistor within the silicon dioxide beneath the gate: The value of this current is in increasing because the gate oxide thickness is reduced to less than 90Å, by this reduction; the value of the leakage current is increasing at the value where it becomes important and could not be ignored. This means that the thinner the gate oxide the higher the gate leakage, this is happening to keep the transistor at the highest rate of speed to obtain the required performance.

The second type of leakage, sinks from the Source to Drain even the transistor remains at the cut off region; so $V_{gs} = 0$, the length of gate which is the distance between the source and the drain is the main factor to prevent this type of current, unfortunately for less than 90nm technology and threshold voltage is less than 0.12V, it becomes very difficult to prevent as shown in Figure1.

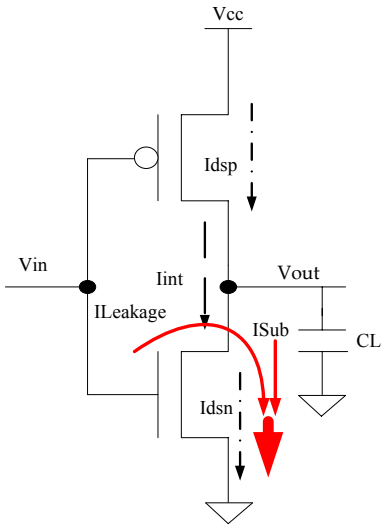


Figure 1: Resources of Leakage Current

Giving an example of 90nm technology, simulation results shown the leakage power dissipated by Pentium IV is the same as the dynamic power dissipation (50% Dynamic Power Dissipation and 50% Leakage power Dissipation). Furthermore, by 2010, the expected value of the leakage current could achieve 75% from the total power dissipation in one single chip as shown in Figure 2[5].

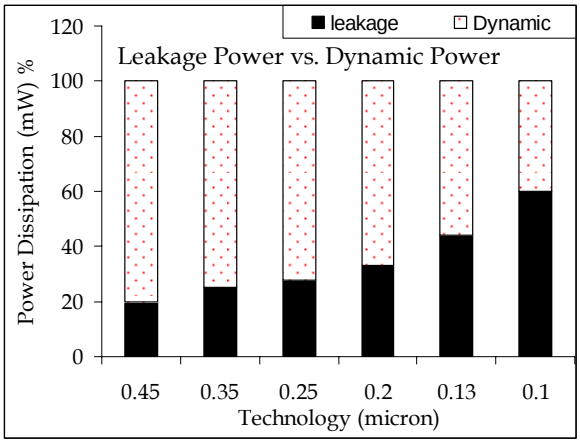


Figure 2: Leakage Current vs. Dynamic Power

Various techniques are approved as efficient methods to decrease the leakage current at transistor level [1][2][3]. In [4] an efficient technique is suggested showing the influence of the gate's length as well as the threshold voltage on the leakage current. In [5] special software package tool is given to measure the leakage current in circuit level. While in [6] the leakage current appearance at the gate level is discussed and analyzed in detail.

In this paper, we implemented a special CAD-tool to calculate the value of leakage current at SPICE level, the proposed approach based on modifying automatically the values of the SPICE parameters which influence the value of the leakage current. We attempt so that the value of the leakage current stay at the minimal value. Simulation results using MATHIMATICA software package tool approved the validity of the proposed technique.

Leakage current appears when a single transistor is in the cut-off region, this means, even the transistor is not at the operational mode, power is dissipating and loosing. Taking in mind the Moore's Law [6] which shows the number of transistors is increasing exponentially by the time from one hand, and the number of transistors at last microprocessor which contains hundreds of millions of transistors from the other hand, where most of time these transistors are in the ideal mode, this will make the value of the leakage current very large, and might exceed

any expected value in the nearest future and remains the main factor of power dissipation for next decade.

In the following paragraphs, we mention the main efficient techniques that reduce the leakage current, and finally we give our approach.

### 2.1 Topology of Transistor

In general, CMOS logic family contains from pull-up and pull-down blocks, the pull-up block contains from pMOS transistors while the pull-down contains from nMOS transistors. When the structure of pMOS transistors is in parallel, the structure of nMOS transistors should be in series and vise versa. Simulation results show that the nearest transistors to the supply voltage are the most ones dissipate leakage current when they are in off state. This is because the $V_{gs}$, becoming negative and high, to avoid this fact, new transistor should be connected in series with the original ones so that the value of its $V_{ds}$ will be decreased to $V_x$ which its in fact lower than the $V_{gs}$ of the first transistor $V_x < V_{gs}$ taking in mind the influence of the body effect[2], in general the $V_x$ could be approximately equal to

$$V_x \cong \frac{\lambda_d V_{CC} + S \log \frac{w_{g1}}{w_{g2}}}{1 + 2\lambda_d} \qquad (1)$$

Where λ is the drain-induced barrier lowering factor (DIBL), $V_{cc}$ is the supply voltage, $S$ is subthreshold swing, $w$ is the width of transistor's gate of upper and lower transistor.

Figure 1.a shows the topology of transistors, while figure 1.b shows the leakage current in both cases. From this point, it is preferable to re-arrange the design so that we modify the parallel transistors connected to the supply voltage by series transistor, so that the value of the leakage current to be at minimum value. This could be happened following the De-Morgan's Laws[6].

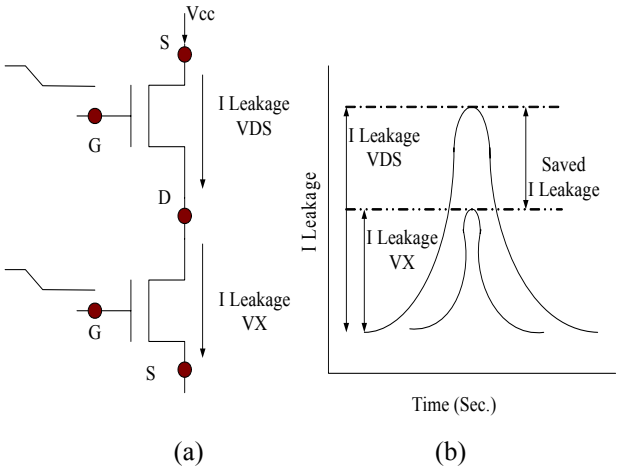


**Figure 1:** a: Two MOS transistors in Series, (b) Leakage Current

### 2.2 Multi-threshold Voltage Technique

An efficient technique to reduce the power dissipation in general and the leakage current in specific is Multithreshold voltage technique. In this case, the circuit consists from two types of transistors: Transistors with high threshold voltage which are located in non-critical path of circuit to prevent the path of the leakage current from the supply voltage to the ground in standby mode, and the other type is transistors with low threshold voltage which are asserted in critical path to keep the circuit at high speed. During the operational mode, transistors with high threshold voltage switches are turned on which makes the transistors with low threshold voltage to operate fast [7]. Figure 2 shows the concept of multithreshold voltage and its application.

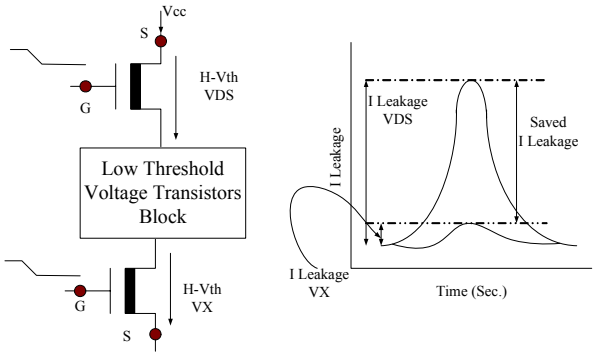


**Figure 2:** Multithreshold Voltage Technique and its Leakage Current.

### 2.3 SPICE Parameters and the leakage Current

The most efficient technique to reduce the dynamic power dissipation is the reduction of the supply voltage. Unfortunately, reducing the supply voltage is the main factor of reduction the speed operation of the circuit. So, in order to keep the speed operation at maximum rate, the threshold voltage and the length of gate should be reduced also.

The reduction of the threshold voltage and length of gate produce increasing of subthreshold voltage leakage currents as shown from the equation 2.

$$I_{subthreshold} = I_o \times 10^{\frac{[V_{gs}-V_t]}{S}} \qquad (2)$$

Giving the shape of transistor in mind and re-calculate the leakage current again according to the width of transistor, the subthreshold leakage current will be increased and the value of the leakage current will be modified to:

$$I_{subthreshold} = \frac{I_o}{W_o} \times W \times 10^{\frac{[V_{gs}-V_t]}{S}} \qquad (3)$$

Where

$$I_o = \mu_o C_{ox} \frac{W}{L} V_{th}^2 e^{1.8} \qquad (4)$$

and $S = nV_{th} \times ln10$.

The $I_o$ is the initial current at the drain of transistor when the voltage between the gate and the source $V_{gs}$ is equal the value of the threshold voltage ($V_{gs}$=$V_t$), $V_t$ is the threshold voltage of transistor, and $S$ is the subthreshold slop. As shown from the above equation, the main parameter which it's the leakage current depends on, is the threshold voltage and the width of transistor. According to the recent technologies, both the threshold voltage and width of transistor are scaling continuously, causes an increasing at the value of the leakage current exponentially, it's also clear that the value of the leakage current could be increased if the value of the $V_{gs}$ is increased too. At the same time, the value of the leakage current could be decreased if the value of $V_{gs}$ decreased also. This could be happened by raising the source voltage which it is out of calculations.

## 3. Proposed Technique

The basic two techniques that play main role in reducing the leakage current are the topology of transistors and Multithreshold voltage transistor, both of them based on SPICE parameters as is from industry without any changes.

Scaling the main SPICE parameters which influence the value of leakage current, each one independently is not the most efficient method to optimize the leakage current value. Otherwise the optimal value of leakage current will be reduced each time we scale any other parameter.

Our approach is based on scaling all these parameters together until we find the lowest value of the leakage current. This could be happened if we take the equations of the leakage current with their parameters and scaling them on the same time. This method will be continued until we find the intersection nodes between those parameters. The correspondence value of leakage current on that node should be the optimal value of the leakage current.

Bellow is the pseudo code illustrates the main approach:

```
FOR each technology DO
Give all SPICE parameters that influence the Leakage:
Read Z
FOR J  =1 TO Z DO
      FOR I = 0 TO MAX DO
     Value[I][J]=Leakage Equation(J)
FOR I =1 TO Max DO
Find all intersection node(s) between SPICE parameters so that the value of the leakage is the same.
```

In order to show the efficiency of this approach, and its influence at the delay time and the power dissipation, the old values will be replaced by the new values and re-run the same technology over the basic logic gates such as INV, OR, AND, NAND and NOR, using the same technology with old and new parameters.

According to our approach the power dissipation is sure decreased as indicated by the pseudo code above. Reference to the delay time its easy to show it when we design in two different files the same logic gates using the two different values of the same technology.

Simulation results using MATHIMATICA package tool shown the new value of the leakage current is reduced in any case, the value of the leakage current should be the minimal value that could be reduced in any case as shown from Figure 4. The crossed points at each figure shows the optimal value of the specific SPICE parameters where the correspondence value of leakage current is the minimum value.

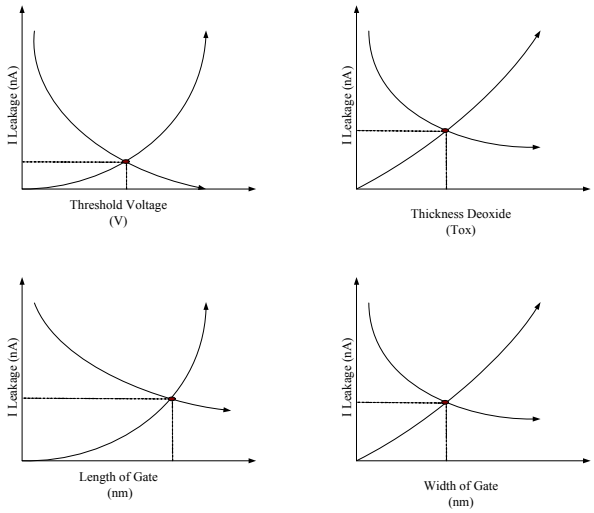


**Figure 4:** Output of the proposed idea for threshold voltage and Thickness Dioxide

It is obvious that for any next generation nano-technology SPICE parameters, the optimal values of their parameters should be known at the first step of SPICEs manufacturing.

## 4. Conclusion

A new approach to find the optimal value of leakage current for next generation technologies is discussed in this paper. The new approach based on calculates the specific value of SPICEs parameters so that the correspondence value of the leakage current is at minimal value. Simulation results approved the validity of the proposed idea.

## *References*

[1] James Kao, *et al*, "subthreshold Leakage Modeling and Reduction Techniques,"

[2] S. Narendra, *et al.* "Full-chip Sub-threshold Leakage Power Prediction Model for sub-0.18 μm CMOS," Intl. Symp. Low Power Electronics and Design, August 2002, pp. 19-23.

[3] S. Narendra, *et al.* "Scaling of Stack Effect and its Application for Leakage Reduction," Intl. Symp. Low Power electronics and Design, August 2001, pp. 195-200.

[4] M. Johnson, D. Somasekhar, L. Chiou, K. Roy, "Leakage Control with Efficient Use of Transistor Stacks in Single threshold CMOS," IEEE Transactions on VLIS Systems, vol. 10, no. 1, , February 2002, pp. 1-5.

[5] Jun Cheol Park, "Sleepy Stack: a New Approach to Low Power VLSI Logic and Memory," Ph. D. thesis, Georgia Institute of Technology, August 2005.

[6] S. Mukhopadhyay and K. Roy, “Accurate Modeling of Transistor Stacks to Effectively Reduce Total Standby Leakage in Nano-scale CMOS Circuits,” VLSI Circuits, Dig. of Tech. Papers, 2003, pp 53-56.

[7] Grove, A.S.: ‘Changing vectors of Moore’s law’. Keynote speech, Int. Electron Devices Meeting, Dec. 2002.