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Temperature Aware Design for High Performance Processors

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Abstract*—efficient temperature aware design in modern microprocessors, especially in the design of digital portable, notebook, and handheld computers is becoming increasingly important. Many studies have been done on microprocessor's dynamic thermal management techniques and methodologies; from thermal estimation to voltage scaling, clock gating, and total/active power monitoring and control. As technology, moves into deep submicron feature sizes and the leakage power are expected to increase because of the exponential increase in leakage currents with technology scaling. In nanometer technologies, it is observed that leakage power will become comparable to dynamic or total power dissipation in the next generation processors in the next few years. This paper presents a hardware design for dynamic thermal management strategies for microprocessors leakage power control, which is particularly appealing for portable and embedded systems. LTspice simulation program is used to verify the theoretical idea and confirm the design operations. Results shows that, the appropriate thermal management system can be designed for a much lower maximum power rating with minimal performance impact for typical applications, considerable amount of power consumption reduction as well as thermal aware challenges have been obtained.

Keywords— Thermal Management, Leakage Power, Reverse Body Biasing.

I. INTRODUCTION

Through past two decades, microprocessor performance has matured about one thousand, delivering extraordinary computing capabilities[1]. The evolution in microprocessor performance has predominantly be driven by the regular scaling of the transistor process featuring that expedites capacity of exponential transistor integration. In other words, the number of transistors in a dense integrated circuit doubles approximately every two years according to Moor's law. Increase in device count per chip and shrinkage of feature size are shown in Fig. 1 [2,3]. More than one-million fold increase in the device count has been achieved these 40 years leading to almost the same increase in processor performance. Whenever transistor density increases, the power density in the microprocessors has also extended exponentially [3]. Further, this power, which is consumed by a microprocessor or integrated circuits, is dissipated as heat due to the resistive behaviour of the Complementary Metal Oxide Semiconductor (CMOS) circuits. High temperature has an adverse effect on many perspectives of microprocessors, such as transistor performance, power consumption and system reliability.

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There are Two main components of power dissipation in CMOS circuits, as described in equation (1) [4].

$$P = P_{dynamic} + P_{leakage} \quad (1)$$

Where P is the total power dissipation, $P_{dynamic}$ is the dynamic power, and $P_{leakage}$ is the static/leakage power.

Lowering power supply voltage is one of the effective schemes to reduce the power dissipation. A number of methods have been proposed to scale down the power supply voltage d

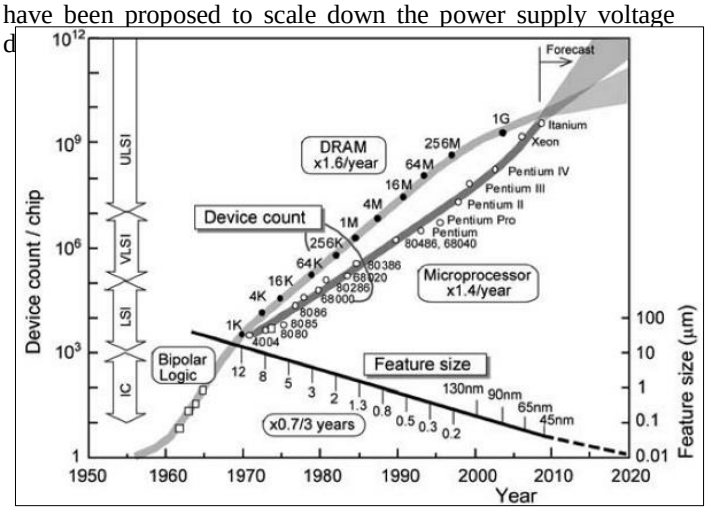

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Fig. 1. Trends in device count/chip and feature size of MOS device

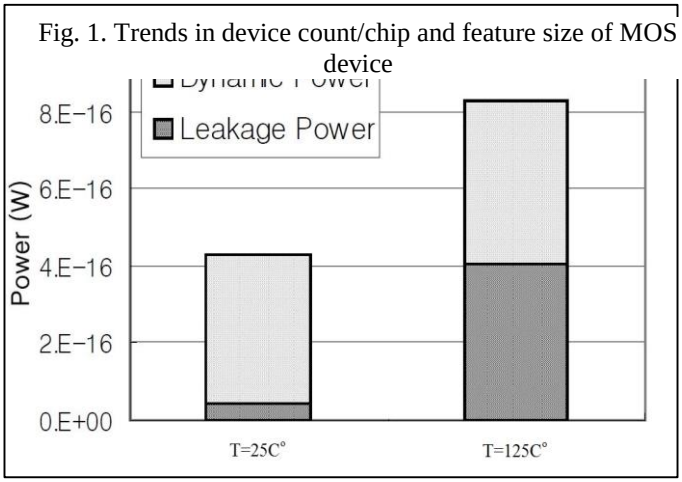

Fig. 2. Dynamic and leakage power of CMOS inverter for different temperatures using the 70nm technology

Even though they are effective in decreasing dynamic power dissipation, it does not help reducing the leakage power effectively, which is the most responsible source for generating heat in CMOS circuits. The non-ideal off-state/leakage characteristic, or a finite resistance, of MOSFETs, current drawn from a power supply even when a transistor operates in the cutoff region. This makes microprocessor and CMOS circuits to consume a power even when they are in standby mode, which is a leakage/static power. Fig. 2 shows the dynamic and leakage power of a 70nm inverter for different operating temperatures. The leakage power, which was initially 10% of the total power at room temperature, increases up to 49% as the temperature goes up to 125C°[6].

As transistor geometries are shrunk aggressively, threshold voltage decreases to achieve high performance resulting in exponential increase in leakage current. Due to the continued scaling of technology, supply and threshold voltage, and leakage, power has become dominant in the power dissipation of nanoscale CMOS circuits. Therefore, optimal power dissipation for a given performance depends not only on power supply voltages but also on the device threshold voltage [7].

To effectively limit the high temperature and reduce the leakage power with a cost-effective, threshold voltage has to be increased in circuit level, by designing a dynamic hardware controller. Body biasing is a low power/thermal management technique used in microprocessors and CMOS digital circuits. It offers an optimum solution for the CPU power/thermal problems by CMOS transistors during modifying circuit operation or program execution. This work uses a reverse body biasing technique for controlling the temperature of microprocessor.

The models and techniques of minimizing dissipated power and generated temperature/thermal variation of a high performance modern CMOS processor are underway, and it has prompted a new research area and in low-power in conjunction with low temperature techniques. Such as, analysis of thermal dynamics in multicore systems, focusing on time response to heat generated in a single core and its connection with very large scale integration (VLSI) design principles that's presented in [8]. Qikai Chen in [9] stabilized the chip temperature by online monitoring using temperature sensor. The proposed circuits in [10] and [11] adaptively adjust the body bias to its optimal value during the whole standby period, which result in considerable reduction of leakage power and effective compensation of process and temperature variations. . Nikhil Saxena and Sonal Soni in [23] present that circuit level techniques incorporated requiring support from technology and process level techniques can be more effective in reducing leakage, where they used stacking effect to reduce leakage current for different input vectors for a stack of 3 Nano technology NMOS transistors. Designs of Forward Body Biased Adiabatic Logic for reduction of average, peak, and differential power have been presented in [24]; this body biasing method was applied to adiabatic Toffoli and Fredkin gates. The designs improved over their non-body biased implementation in all power metrics, as well as improved output signals. The designs improved the differential power over conventional NAND and MUX gates.

In order to ensuring low power operation for efficient power and temperature aware design for modern microprocessors, this work tries to study, design, and simulate the temperature aware controller based on dynamic frequency scaling. Where this controller adjust the threshold voltage of NMOS transistors within the microprocessor by sensing it's temperature, then generating frequencies matching the frequency of the microprocessor to make the controller respond to the change in temperature with a quickness proportions of the microprocessor's speed. Resulted frequency will actuate the controller to produce a voltage, which is reverse body bias voltage (V_{body}).

II. EFFECT OF BODY BIASING ON THRESHOLD VOLTAGE, LEAKAGE COMPONENTS AND TEMPERATURE

The threshold voltage is typically adjusted and accommodated during the fabrication process by varying the doping concentration in the channel area [12]. Alternatively, the body bias circuit technique utilizes the body terminal to dynamically modify the threshold voltage of a transistor during circuit operation. Depending upon the polarity of the voltage difference between the source and body terminals (VSB), the threshold voltage can be either increased or decreased as compared to a zero body biased transistor. The threshold voltage is increased when the source-to-substrate p–n junction of a MOSFET is reverse biased. The threshold voltage of a MOSFET can also be reduced by forward biasing the source-to substrate p–n junction [13]. Among the leakage power reduction techniques, RBB technique, which increases the threshold voltage (Vth) of transistors and are extensively employed to suppress the sub-threshold leakage current (ISUB) as depicted in Figs. 3 and 4 [14,15].

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However, this technique also aggravates short channel effects (SCEs), such as drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL), and band-to- band tunneling (BTBT) current. In particular, GIDL and BTBT current significantly increases under the reverse body bias condition since the state-of-the-art MOSFETs are fabricated with high overall doping concentrations, lowered source/drain junction depths, halo doping, high-mobility channel materials, etc.

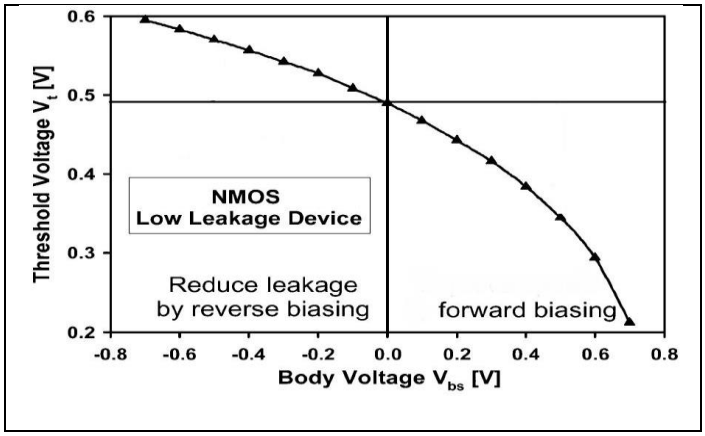

Fig. 3. Body bias effect on threshold voltage in 90-nm CMOS technology

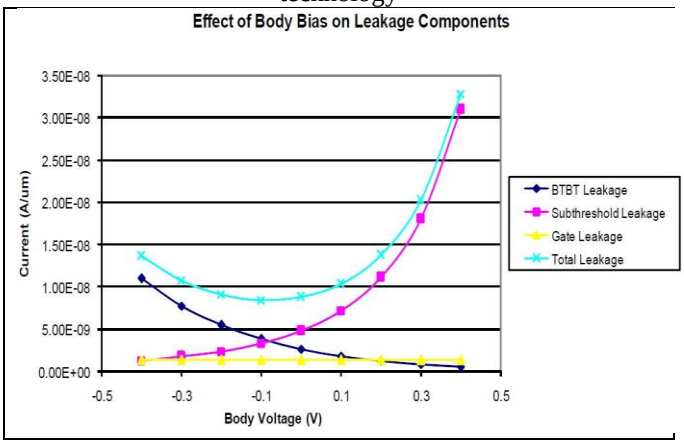

Fig. 4. Effect of body bias on leakage components for a 70nm predictive technology

Furthermore, the reduction of the gate oxide thickness (tox) causes a drastic increase in the gate tunnelling leakage current due to carriers tunnelling through the gate oxide, which is a strong exponential function of the voltage magnitude across the gate oxide [16,7].

When the gate-to-source voltage in a MOS transistor is below Vth, the transistor is not completely turned off, instead, there is weak inversion region having some minority carriers along the length of the channel.

This makes a small current flow from drain to source in NMOS case, which is called the sub-threshold leakage. ISUB is the component that affected by temperature and threshold voltage. This current can be expressed based on [14]:

$$I_{SUB} = \mu C_{dep} \frac{W}{L} V_T^2 \left(exp \frac{V_{GS} - V_{th}}{nV_T} \right) \left(1 - exp \frac{-V_{DS}}{V_T} \right) \qquad (2)$$

Where Cdep = $\sqrt{\varepsilon siqN sub/(4\emptyset B)}$ denotes the capacitance of the depletion region under the gate area, $\boldsymbol{\varepsilon}$si is the permittivity of Si, q is the electron charge, $\boldsymbol{N}$sub is the doping concentration of the p-substrate, ØB is the built-in potential, VT is the thermal voltage that is equal to kT/q, Cox is the oxide capacitance per unit area between the gate metal and the bulk surface, and n is the sub-threshold parameter and is expressed as 1 + Cdep/Cox.

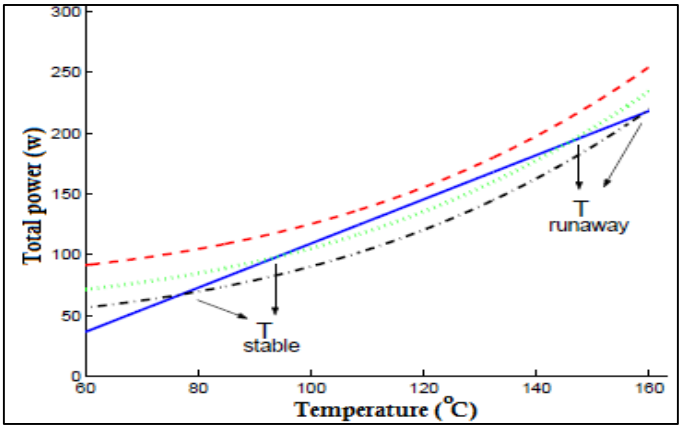

Fig. 5. The power-temperature thermal runaway

From the above equation that the positive feedback loop between power dissipation and temperature is seen i.e., increasing the temperature will increase the leakage current and increased leakage current will further increase the temperature. Higher generated temperatures lead to higher dissipated leakage and total power, therefore thermal runaway will occur when the rate of temperature generation becomes greater than the rate of heat removal [15].

Power-temperature thermal runaway will become more critical in future technologies.

Fig. 5 shows that, the thermal runaway is a destructive positive feedback condition that can occur when inadequate thermal control is combined with a silicon process technology where the leakage increases the current exponentially with the generated temperature.

III. CONTROLLER IMPLEMENTATION

The specific controller implementation of the proposed technique is shown in Fig. 6. The temperature of the microprocessor chip will be directly converted to a frequency, which match the frequency of the desired microprocessor or CMOS chip. After that, the phase locked loop (PLL) will process this frequency to generate the RBB voltage.

In microprocessors, the non-uniformity of power consumption can cause a much higher local power density. Those regions on the die with a high temperature called hotspots. Temperature in the hotspots rise much faster than the full chip; therefore, they could be utilized for temperature sensing by using temperature sensors [16]. A voltage signal will be

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generated by temperature monitoring circuit and the value of voltage signal will increase proportionally with temperature [9].

To make the controller system operate with accurate response, the incoming voltage from temperature sensor has to be converted to a higher frequency, matching the frequency of the desired microprocessor. To achieve this purpose, voltage control oscillator (VCO) could be used [17]. After that the temperature is converted to frequency by temperature monitoring circuit, VCO and frequency divider, PLL shown in Fig. 6. will be driven by this frequency to generate a voltage, which is the voltage at the output of the loop filter within PLL.

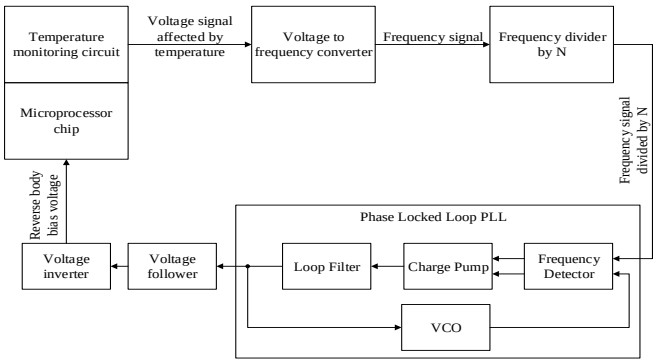


Fig. 6. Block diagram of temperature controller unit

This voltage will be the desired reverse body bias voltage that has been used to decrease leakage power/temperature of microprocessor or CMOS chip.

IV. SIMULATION RESULTS

Based on specification of microprocessor and it's temperature usage levels, the controller computes the required V_{body} to be applied on the bodies of NMOS transistors within CPU. This means that, the temperature control unit is the power controller such that leakage power consumption and generated heat at a particular operating frequency are minimized. Table 1 shows the temperature usage levels of Intel® Core™ i3-3217U 1.80 GHz Processor (which is one of the modern microprocessor produced in recent years) [18].

By applying the controller on the mentioned CPU, the temperature control unit will be activated just when the temperature reaches maximum range, otherwise the controller will be in idle state. Jing Yang and Yong-Bin Kim approve that the optimal value of RBB is 0.38 [19], therefore in this work we will consider this value as a maximum value of RBB voltage generated by temperature controller unit. The maximum temperature range will be divided to three ranges to generate three values as presented in table 2.

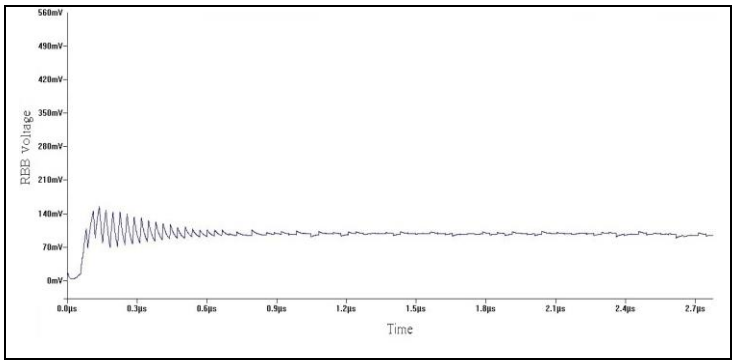
Table 2 confirms that the generated frequency identify the frequency of the desired CPU. Fig. 7. shows the simulation results of the controller for the three cases.

Table 1 Intel® Core™ i3-3217U temperature levels

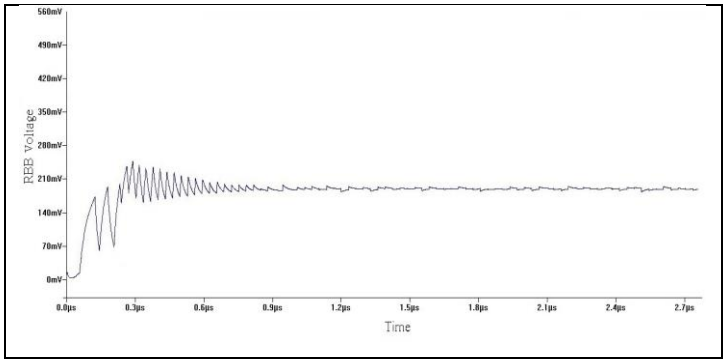
Idle temperature	Normal temperature	Maximum temperature
34 to 49 °C	50 to 60 °C	61 to 75 °C

Table 2 Desired value of temperatures for the controller

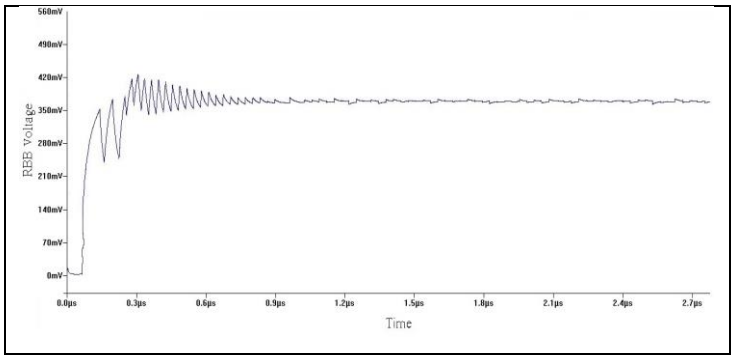
Temperature range	VCO frequency	RBB voltage
61 to 65 °C	1.6 GHZ	0.1 V
66 to 70 °C	1.7 GHZ	0.2 V
71 to 75 °C	1.8 GHZ	0.38 V



(a)



(b)



(c)

Fig. 7. RBB voltage with time for: (a) 61 to 65 °C; (b) 66 to 70 °C; (c) 71 to 75 °C;

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By applying, those values of RBB voltage on a single CMOS inverter, leakage current and temperature will be decreased significantly. Fig. 8. shows the effect of RBB voltage on leakage current for different temperature ranges.

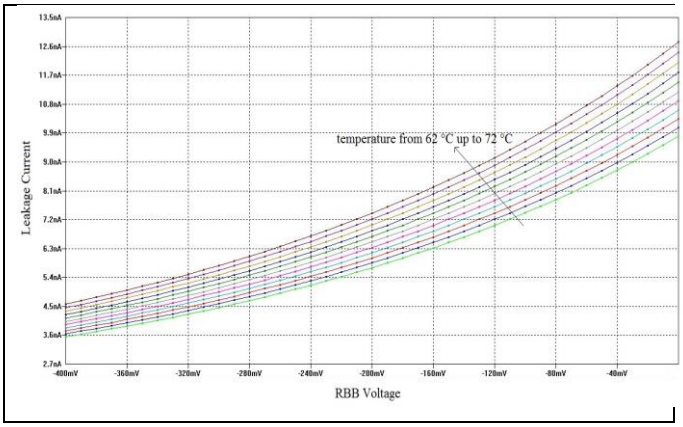

Fig. 8. Effect of RBB voltage on leakage current of a CMOS inverter using 50nm technology I for different

V. CONCLUSION

Thermal management is one of the many crucial tasks in the design of high performance processors/CMOS chips. Current processor's design challenges in portable and embedded systems becoming more complex and high transistor's count, both thermal management and power consumption reduction is becoming significant in the design process. Therefore, improving microprocessors power and temperature have been the primary consideration in digital VLSI design; many researches are now underway on minimizing power dissipation and operating temperature reduction, especially for portable and high performance systems. In portable systems where processor circuits spend most of their time in an idle state with no computation, to maintain both the processor's supply voltage and clock frequency, thermal reduction technique has emerged as an effective way for minimizing energy consumption as well as low temperature designs. In this study, a temperature control unit was designed and simulated using LTspice simulator for different temperatures' and it was confirm that, the controller generates the desired values of RBB voltage for different temperature ranges; those values were applied for a single CMOS inverter, using 50nm technology.

It was clear that the controller decreased the leakage current significantly, and because of the direct proportionality between leakage current and temperature, the temperature was automatically detracted.

Therefore, the temperature aware technique confirms superiority on leakage power consumption reduction as well as temperature reduction mechanisms, and it shows the good promises in processor's thermal-energy optimization. Therefore, it is possible to integrate and use the thoughts of this technique with any existing processor to study system level power and thermal issues for various high performance processors accurately.

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